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HW #4

1. A)

Assume: Only one valid state at a time

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Core | Request Type | C0 Cache Line State | C1 Cache Line State | C2 Cache Line State | C3 Cache Line State |
| 1 | 0 | Read x | Valid | - | - | - |
| 2 | 1 | Read x | Invalid | Valid | - | - |
| 3 | 2 | Read x | Invalid | Invalid | Valid | - |
| 4 | 3 | Write x | Invalid | Invalid | Invalid | Valid |
| 5 | 1 | Read x | Invalid | Valid | Invalid | Invalid |

B)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Core | Request Type | C0 Cache Line State | C1 Cache Line State | C2 Cache Line State | C3 Cache Line State |
| 1 | 0 | Read x | Shared | - | - | - |
| 2 | 1 | Read x | Shared | Shared | - | - |
| 3 | 2 | Read x | Shared | Shared | Shared | - |
| 4 | 3 | Write x | Invalid | Invalid | Invalid | Modified |
| 5 | 1 | Read x | Invalid | Shared | Invalid | Shared |

C)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Core | Request Type | C0 Cache Line State | C1 Cache Line State | C2 Cache Line State | C3 Cache Line State |
| 1 | 0 | Read x | Exclusive | - | - | - |
| 2 | 1 | Read x | Shared | Shared | - | - |
| 3 | 2 | Read x | Shared | Shared | Shared | - |
| 4 | 3 | Write x | Invalid | Invalid | Invalid | Modified |
| 5 | 1 | Read x | Invalid | Shared | Invalid | Shared |

2)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Core | Request Type | Address | C0  L1 State | C1  L1 State | C2  L1 State | C3  L1 State |
| 1 | 0 | Load | 0x00ffabc0 | E | - | - | - |
| 2 | 0 | Store | 0x00ffabc8 | M | - | - | - |
| 3 | 1 | Load | 0x00ffabc4 | S | S | - | - |
| 4 | 1 | Store | 0x00ffabc8 | I | M | - | - |
| 5 | 1 | Load | 0x00afabc0 | - | E | - | - |
| 6 | 2 | Load | 0x00afabc8 | - | S | S | - |
| 7 | 1 | Load | 0x00bfabc0 | - | E | - | - |
| 8 | 0 | Load | 0x00ffabc0 | E | - | - | - |

3)

Number Of Pages: 2^40 bytes, 2^14 size.

(2^40)/(2^14) = 2^26 = 67108864 Pages

Max Size Of Addressable Physical Memory: 4 byte entry which means we can represent 2^32 pages. Size of one page is 2^14.

(2^32) \* (2^14) = 2^46 Bytes

Size Of a One-Level Page Table: 2^26 pages, 2^2 bytes per page table entry

(2^26) \* (2^2) = 2^28 Bytes

Size Of a Two-Level Page Table: Divide the virtual address into 14 ,13 and 13

(2^33)/(2^14) = 2^19 pages

(2^19)/(2^13) = 2^6 13 bit chunks

(2^14 \* 4) + (2^6 \* 2^13 \* 4) = 2^21+2^16 Bytes

Bonus)

A)

4KB:

# Of Entries For Each Program:

Virtual Address Space: 2^28 bytes

Page Size = 2^12 bytes

(2^28)/(2^12) = 2^16 page entries

Total Page Table Size:

Virtual Address Space: 2^28 bytes

Page Size = 2^12 bytes

(2^28)/(2^12) = 2^16 pages

2^16 \* 4 = 262144 bytes for table size

16KB:

# Of Entries For Each Program:

Virtual Address Space: 2^28 bytes

Page Size = 2^14 bytes

(2^28)/(2^14) = 2^14 page entries

Total Page Table Size:

Virtual Address Space: 2^28 bytes

Page Size = 2^14 bytes

(2^28)/(2^14) = 2^14 pages

2^14 \* 4 = 65536 bytes for table size

B) 4 Bit Tag & 12 Bit Offset

|  |  |  |  |
| --- | --- | --- | --- |
| Valid | Tag | Physical Address | LRU |
| 1 | 0x3 | 0x13 | 7 |
| 1 | 0xF | 0x1F | 4 |
| 1 | 0x8 | 0x18 | 5 |
| 1 | 0x0 | 0x10 | 6 |

0x6D10 TLB Hit

0x9000 TLB Miss & Page Table Fault

0xF200 TLB Hit

0xF800 TLB Hit

0x8800 TLB Miss & Page Table Fault

0x0000 TLB Miss & Page Table Fault

0x3100 TLB Miss & Page Table Fault

C) 3 Bit Tag & 1 Bit Index & 12 Bit Offset

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Valid | Tag | Index | Physical Address | LRU |
| 1 | 0x0 | 0 | 0x10 | 3 |
| 1 | 0x4 | 0 | 0x14 | 2 |
| 1 | 0x1 | 1 | 0x11 | 4 |
| 1 | 0x7 | 1 | 0x17 | 3 |

0x6D10 = 011 0 D10 TLB Miss & Page Table Fault

0x9000 = 100 1 000 TLB Miss & Page Table Fault

0xF200 = 111 1 200 TLB Miss & Page Table Fault

0xF800 = 111 1 800 TLB Hit

0x8800 = 100 0 800 TLB Miss & Page Table Fault

0x0000 = 000 0 000 TLB Miss & Page Table Fault

0x3100 = 001 1 100 TLB Miss & Page Table Fault

D) 2 Bit Tag & 2 Bit Index & 12 Bit Offset

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Valid | Tag | Index | Physical Address | LRU |
| 1 | 0x0 | 00 | 0x0 | 2 |
| 1 | 0x2 | 01 | 0x12 | 1 |
| 1 | 0x1 | 10 | 0x11 | 1 |
| 1 | 0x0 | 11 | 0x10 | 3 |

0x6D10 = 01 10 D10 TLB Miss & Page Table Fault

0x9000 = 10 01 000 TLB Miss & Page Table Fault

0xF200 = 11 11 200 TLB Miss & Page Table Fault

0xF800 = 11 11 800 TLB Hit

0x8800 = 10 00 800 TLB Miss & Page Table Fault

0x0000 = 00 00 000 TLB Miss & Page Table Fault

0x3100 = 00 11 100 TLB Miss & Page Table Fault

E) 2 bit tag, 14 bit offset

|  |  |  |
| --- | --- | --- |
| Valid | Tag | Physical Address |
| 0 | 0x0 | 0x10 |
| 1 | 0x3 | 0x13 |
| 0 | 0x0 | 0x10 |
| 1 | 0x1 | 0x11 |

F)

|  |  |  |  |
| --- | --- | --- | --- |
| Valid | Tag | Physical Address | LRU |
| 0 | 0x2 | 0x12 | 5 |
| 1 | 0x3 | 0x13 | 4 |
| 0 | 0x0 | 0x10 | 7 |
| 1 | 0x1 | 0x11 | 1 |

0x6D10 = 01 10 D10 TLB Hit

0x9000 = 10 01 000 TLB Miss & Page Table Fault

0xF200 = 11 11 200 TLB Hit

0xF800 = 11 11 800 TLB Hit

0x8800 = 10 00 800 TLB Hit

0x0000 = 00 00 000 TLB Hit

0x3100 = 00 11 100 TLB Hit